UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,189	07/02/2003	William P. Wedlake	10018287-1	4151

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EXAMINER
COUGHLAN, PETER D

ART UNIT	PAPER NUMBER
2129	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/612,189	WEDLAKE ET AL.
	Examiner	Art Unit
	Peter Coughlan	2129

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 July 2003</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-44</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-44</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>02 July 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some.* c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Detailed Action

1.   Claims 1-44 are pending in this application.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 3, 8, 13, 17, 18, 20, 24, 25, 28, 33, 37, 38, 40, 44 are rejected under

35 U.S.C. 102(e) (hereinafter referred to as **Henderson**) being clearly anticipated by

Henderson et al., U.S. Patent 5602536.

Claims1, 24 and 44.

Henderson teaches one or more analyzers which govern the analysis of specific

configuration information to determine whether the software and/or the hardware

associated with a node and/or a group of nodes is configured properly (**Henderson**,

C22:1-4; Examiner's Note (EN) 'Analyzer' of applicant is equivalent to 'CPU' of

Henderson. 'Node' of applicant is equivalent to 'flag' of Henderson.); one or more

analyzers which govern the analysis of specific information resulting from testing to

determine whether the tested software and/or hardware associated with a node and/or a group of nodes is functioning properly (**Henderson**, C22:2-18); one or more analyzers which govern the analysis of specific diagnostic and/or log information to determine whether the software and/or the hardware associated with a node and/or a group of nodes is functioning properly (**Henderson**, C36:8-13); and these analyzers also govern the determination of whether and, if so, of what specific issue information is to be produced. (**Henderson**, C15:5-8; EN 'Error message' of Henderson is equivalent to 'issue information' of applicant.)

Claims 2 and 25.

Henderson teaches a harness or framework which, when provided with a list of one or more of the analyzers and with a list of one or more nodes or groups of nodes, exercises one or more of the analyzers against specific data associated with each node or group of nodes, captures any issue information produced, and augments such issue information with node identification information to produce an issues database. (**Henderson**, C221-18 & C18:43-48; EN Henderson illustrates a framework in which analyzers (CLU) with nodes (flag of Henderson) against specific data (RAM of Henderson) to capture issue information (corrupted of Henderson) to produce an issue database (diagnostic maintenance log of Henderson))

Claim 3.

Henderson teaches at least some analyzers include a code portion and a

descriptor portion, the descriptor portion containing information identifying at least some

of the specific node information required for the performance of the analysis defined by

the code portion. (**Henderson**, C22:1-18; EN 'Code portion' and 'descriptor portion' of

applicant is equivalent to 'characterization instructions' and 'software switch' of

Henderson.)

Claims 8 and 28.

Henderson teaches analyzing the configuration of service guard or equivalent

software which software performs functional analyses of at least one mission critical

switch guard or equivalent node cluster and which software switches one or more tasks

from node to node within such a cluster to keep mission critical tasks running.

(**Henderson**, C22:4-8)

Claims 13 and 33.

Henderson teaches analyzing system logging file entries. (**Henderson**, C4:56

through C5:7; EN 'Analyzing system' of applicant is equivalent to 'operations that are

executed' of Henderson.)

Claims 17 and 37.

Henderson teaches analyzing data indicating whether the service guard related

daemons or their equivalents are operating properly to insure the continuance of

mission critical tasks. (**Henderson**, C22:1-8; EN 'Daemons' of applicant is equivalent to

'master software switch'.)

Claims 18 and 38.

Henderson teaches analyzing the operational status of at least one service guard

or equivalent cluster of nodes, signaling an issue if such a cluster is down, or if one or more

tasks of such a cluster is not running, or if no alternative node is available to which *one*

or more tasks may be switched. (**Henderson**, C22:45-54; 'Operational status' and

'signaling an issue' of applicant is equivalent to detecting and issuing an error of

Henderson.)

Claims 20 and 40.

Henderson teaches at least one analyzer which data relating to the CPUs to

determine if any have been de-configured. (**Henderson**, C22:8-18; EN 'De-configured' of

applicant is equivalent to 'corruption' of Henderson.)

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed
> or described as set forth in section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are such that the subject
> matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7, 9-12, 14-16, 19, 21-23, 26, 27, 29-32, 34-36, 39, 41-43 are rejected

under 35 U.S.C. 103(a) as being unpatentable over McDonald et al in view of

Maity, and further in view of Rowan,

and further in view of Lee, and further in view of Gill and further in view of

Nagamasa and further in view of Griesinger (U. S. Patent 6053951, referred to

as **McDonald**; U. S. Patent 6973587, referred to as **Maity**; U. S. Patent 4893815,

referred to as **Rowan**; U. S. Patent 6202174, referred to as **Lee**; U. S. Patent

6178486, referred to as **Gill**; U. S. Patent 6225911, referred to as **Nagamasa**;

U. S. Patent 6049387, referred to as **Griesinger**).

Claims 4 and 5.

Henderson does not teach at least some analyzers include a code portion and a

template portion, the template portion defining the format of at least some specific issue

information that may be generated as a result of the performance of the analysis

defined by the code portion. McDonald teaches at least some analyzers include a code

portion and a template portion, the template portion defining the format of at least some

specific issue information that may be generated as a result of the performance of the

analysis defined by the code portion. (**McDonald**, abstract & C21:41-54; 'Issue

information' of applicant is equivalent to 'error out' of McDonald.) It would have been

obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Henderson by using templates for standardized output for errors as taught by McDonald to have at least some analyzers include a code portion and a template portion, the template portion defining the format of at least some specific issue information that may be generated as a result of the performance of the analysis defined by the code portion.

For the purpose of having an established output to help users use the system.

Claims 6 and 26.

Henderson and McDonald do not teach analyzing the primary and secondary boot disks of one or more nodes to insure that the boot disks are not installed on the same path and that their configurations are logical. Maity teaches analyzing the primary and secondary boot disks of one or more nodes to insure that the boot disks are not installed on the same path and that their configurations are logical. (**Maity**, C5:31-46 & C9:25-64; EN If there exists more than one primary boot device then there exists a secondary boot device.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson and McDonald by having 2 separate boot systems as taught by Maity to analyze the primary and secondary boot disks of one or more nodes to insure that the boot disks are not installed on the same path and that their configurations are logical.

For the purpose of a reliable boot system that can have multiple boot devices.

Claims 7 and 27.

Henderson, McDonald and Maity do not teach analyzing the standard and backup kernel files of one or more nodes to insure that the kernel files are not installed on the same path and that their configurations are logical. Rowan teaches analyzing the standard and backup kernel files of one or more nodes to insure that the kernel files are not installed on the same path and that their configurations are logical. (**Rowan**, Fig 115d & C82:60-67; EN In figure 115d, the multiple paths are the links between SUBPROGRAM #i to IF COND THEN(i). 'Logical' of applicant is equivalent to 'formmg lemeas or separate and distinct conditional truths' of Rowan.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson, McDonald and Maity by utilizing a primary and secondary kernel files as taught by Rowan to analyze the standard and backup kernel files of one or more nodes to insure that the kernel files are not installed on the same path and that their configurations are logical.

For the purpose of reliable access to the kernel files.

Claims 9 and 29.

The combination of Henderson and McDonald do not teach analyzing the configuration of one or more hardware devices associated with a node or group of nodes. Maity teaches analyzing the configuration of one or more hardware devices associated with a node or group of nodes. (**Maity**, C3:33-36) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify

combined teachings of Henderson and McDonald by detecting faulty hardware to unsure the analyzers are operating within specified parameters as taught by Maity to analyze the configuration of one or more hardware devices associated with a node or group of nodes.

For the purpose of the analyzers to perform the specified function correctly.

Claims 10 and 30.

Henderson, McDonald, Maity and Rowan do not teach analyzing the system dump configurations of one or more nodes to see that the nodes are configured correctly to enable the performance of a successful system dump in case of a system crash or other failure. Lee teaches analyzing the system dump configurations of one or more nodes to see that the nodes are configured correctly to enable the performance of a successful system dump in case of a system crash or other failure. (**Lee**, C1:20-26, C15:32-47 & C6:55 through C7:40; EN C1 illustrates the ability to detect a possible situation, C15 illustrates a cause for a dump, and C6-7 illustrates vents that happen during a dump) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson, McDonald, Maity and Rowan by detecting a possible dump situation as taught by Lee to analyze the system dump configurations of one or more nodes to see that the nodes are configured correctly to enable the performance of a successful system dump in case of a system crash or other failure.

For the purpose of forecasting possible negative results and taking counter

measures.

Claims 11 and 31.

The combination of Henderson, McDonald and Maity do not teach analyzing

memory error indication information from one or more nodes to determine if memory error

conditions are present and, if so, are serious enough to require attention. Rowan

teaches analyzing memory error indication information from one or more nodes to

determine if memory error conditions are present and, if so, are serious enough to require

attention (**Rowan**, C18:3-14 & C73:27-43) It would have been obvious to a person

having ordinary skill in the art at the time of applicant's invention to modify combined

teachings of Henderson, McDonald and Maity by using a threshold to determine if an

error is valid or not as taught by Rowan to analyze memory error indication information

from one or more nodes to determine if memory error conditions are present and, if so,

are serious enough to require attention.

For the purpose of not over reacting to every error signal and react to those

which surpass a given threshold.

Claims 12 and 32.

Henderson, McDonald, Maity, Rowan and Lee do not teach analyzing at least

some data retrieved from a circular *buffer* containing diagnostic information and/or error

messages. Gill teaches analyzing at least some data retrieved from a circular *buffer*

containing diagnostic information and/or error messages. (**Gill**, abstract; EN 'Round robin circular priority arrangement' of Gill is equivalent to 'circular buffer' of applicant.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson, McDonald, Maity, Rowan and Lee by scrolling through processes as taught by Gill to analyze analyzing at least some data retrieved from a circular *buffer* containing diagnostic information and/or error messages.

For the purpose not fixating on one process when there is a limited amout of resources available.

Claims 14 and 34.

The combination of Henderson, McDonald, Maity and Rowan do not teach analyzing an error log of I/O errors. Lee teaches analyzing an error log of I/O errors. (**Lee**, C1:29-41 & C1:61 through C2:10) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson, McDonald, Maity and Rowan by checking the status of the I/O ports as taught by Lee to analyze an error log of I/O errors.

For the purpose of determining if the input or output are a source of problems for the invention.

Claims 15 and 35.

The combination of Henderson, McDonald, Maity and Rowan do not teach analyzing information extracted from CPU hardware logs of each processor installed upon a node. Lee teaches analyzing information extracted from CPU hardware logs of each processor installed upon a node. (**Lee**, C1:29-41 & C1:61 through C2:10) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson, McDonald, Maity and Rowan by checking hardware components for errors as taught by Lee to analyze information extracted from CPU hardware logs of each processor installed upon a node.

For the purpose of determining if a hardware failure is a source of problems for the invention.

Claims 16 and 36.

The combination of Henderson, McDonald, Maity, Rowan and Lee do not teach analyzing disk usage data to determine the likelihood of "disk full" conditions occurring soon. Gill teaches analyzing disk usage data to determine the likelihood of "disk full" conditions occurring soon. (**Gill**, C8:24-35) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson, McDonald, Maity, Rowan and Lee by using the system to determine if a disk is full as taught by Gill to analyze disk usage data to determine the likelihood of "disk full" conditions occurring soon.

For the purpose of looking forward and preventing a "full disk" situation which could lead to slowing down or stopping the system.

Claims 19 and 39.

The combination and Henderson and McDonald do not teach at least one analyzer which analyzes the status of one or more file systems. Maity teaches at least one analyzer which analyzes the status of one or more file systems. (**Maity**, C6:59 through C7:10; 'Analyzes the status' of applicant would occur when the system would go through the 'boot process' of Maity.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to combined teachings of Henderson and McDonald by having the system check the integrity of the file systems as taught by Maity to have at least one analyzer which analyzes the status of one or more file systems.

For the purpose of having a correct identity associated with a file system.

Claims 21 and 41.

Henderson, McDonald, Maity, Rowan, Lee, and Gill do not teach at least one analyzer which analyzes the status of the CPU fans. Nagamasa teaches at least one analyzer which analyzes the status of the CPU fans. (**Nagamasa**, C8:7-14) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify combined teachings of Henderson, McDonald, Maity, Rowan, Lee, and Gill by having the CPU check the status of the cooling fans as taught by Nagamasa to have one analyzer which analyzes the status of the CPU fans.

For the purpose of protecting the system from overheating.

Claims 22 and 42.

The combination of Henderson, McDonald, Maity, Rowan, Lee, and Gill do not
teach at least one analyzer which analyzes the status of the CPU power supplies.
Nagamasa teaches at least one analyzer which analyzes the status of the CPU power
supplies. (**Nagamasa**, C1:21-25) It would have been obvious to a person having
ordinary skill in the art at the time of applicant's invention to modify combined teachings
of Henderson, McDonald, Maity, Rowan, Lee, and Gill by having the CPU react to the
status of the power supply as taught by Nagamasa to have at least one analyzer which
analyzes the status of the CPU power supplies.

For the purpose of the CPU having control that portion of the system to prevent
future damage.

Claims 23 and 43.

Henderson, McDonald, Maity, Rowan, Lee, Gill and Nagamasa do not teach at
least one analyzer which analyzes the output generated by i/o device scans. Griesinger
teaches at least one analyzer which analyzes the output generated by i/o device scans.
(**Griesinger**, C6:31-35) It would have been obvious to a person having ordinary skill in
the art at the time of applicant's invention to modify combined teachings of Henderson,
McDonald, Maity, Rowan, Lee, Gill and Nagamasa by having the CPU give a final
analysis to the output as taught by Griesinger to have at least one analyzer which
analyzes the output generated by i/o device scans.

For the purpose of the output being in an acceptable state.

Conclusion

4.   The prior art of record and not relied upon is considered pertinent to the

applicant's disclosure.

-U. S. Patent 6175955: Ojennes

-U. S. Patent 6148337: Estberg

-U. S. Patent 6107821: Kelem

-U. S. Patent 6038690: Jacobson

-U. S. Patent 5956477: Ranson

5.   Claims 1-44 are rejected.

Correspondence Information

6.   Any inquiry concerning this information or related to the subject disclosure should

be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-

5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45

p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor David Vincent can be reached at (571) 272-3687. Any response to this

office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

Hand delivered to:

Receptionist,

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Randolph Building,

401 Dulany Street,

Alexandria, Virginia 22313,

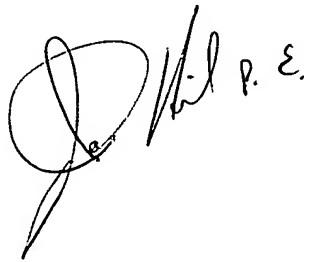(located on the first floor of the south side of the Randolph Building);

or faxed to:

(571) 273-8300 (for formal communications intended for entry.)

Information regarding the status of an application may be obtained from the

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on access to Private PAIR system, contact the Electronic Business Center (EBC) at

866-217-9197 (toll free).

Peter Coughlan

1-12-2006